

Patent Claims

1. A circuit arrangement for protecting integrated  
5 semiconductor circuits from electrical pulses or  
electrical overvoltages, said circuit arrangement  
having
  - an RC element which comprises a first resistor  
(R1; R10) and a capacitance (C1; C10) and is  
10 connected between two supply potential lines (VDD,  
VSS),
  - a chain of inverters (I10 - I12) which are  
connected in series, the input of said chain being  
connected to the junction point between the first  
15 resistor (R1; R10) and the capacitance (C1; C10),  
and
  - having a protection transistor (ST) whose control  
input is connected to the output of the inverter  
chain and whose outputs are connected to the two  
20 supply potential lines (VDD, VSS), characterized  
in that  
the junction points between the inverters (I10 -  
I12) and between the inverters and the protection  
transistor (ST) are each connected to a resistor  
25 (R11, R12, R13), with the respective other  
connection of the resistors being connected to one  
of the supply potential lines (VDD, VSS).
2. The circuit arrangement as claimed in claim 1,  
30 characterized in that  
the resistors are alternately connected to each of  
the supply potential lines (VDD, VSS).
3. The circuit arrangement as claimed in claim 1 or  
35 2, characterized in that  
the input of the last inverter (I12) in the  
inverter chain is connected to one supply

potential line (VDD) via one of the resistors (R11), and the output of the last inverter (I12) in the inverter chain is connected to the other supply potential line (VSS) via another one of the  
5 resistors (R12) and is connected to the control input of the protection transistor (ST).

4. The circuit arrangement as claimed in one of claims 1 to 3, characterized in that  
10 the inverters are in the form of CMOS inverters (P10, N10; P11, N11; P12, N12).
5. The circuit arrangement as claimed in one of claims 1 to 4, characterized in that  
15 the resistors are in the form of diffusion resistances.
6. The circuit arrangement as claimed in one of claims 1 to 5, characterized in that  
20 the first resistor (R10) is a diffusion resistance.
7. The circuit arrangement as claimed in one of claims 1 to 6, characterized in that  
25 the capacitance (C1; C10) is an oxide capacitance.